Document Name	System	Developed for
I400 Version Notes	I400	General Distribution

9/20/2006 FPGA 1.1 PIC 2.0

Problem/Feature	Module	Description
Initial release.		

4/11/2007 FPGA 1.3 PIC 3.0

Problem/Feature	Module	Description
The Rev3 I400 needs to be supported.	FPGA PIC	This version supports hardware revisions 2 and 3 of the I400.
A lock-out condition has been detected when operating in terminal ASCII mode. If the SYSTem:COMMunication:TIMEout is set to a non-zero value the device will disconnect as programmed after the specified elapsed time, causing all commands to be rejected except SYSTem:COMMunication:CONNect. If the timeout was set too low (e.g. 1 second), it is possible that a given host may never be able to write to the device fast enough to connect or to modify the timeout, causing a lockout with the device. This is seen particularly in ASCII terminal mode, where commands are typed in slowly by an operator.	PIC	All system level commands can now be issued while in the not-connected state, including SYSTem:COMMunication:TIMEout. This allows the lock-out condition described to the left to be rectified.
The Rev3 I400 independently turns on the internal calibration source for each channel.	PIC	The command CALIB:SOURce now takes the channel number as the argument (previously was 0 or 1 to disable/enable for all channels). A 0 disables the internal source, a 1-4 sets the source to the specified channel. For I400 hardware revisions under 3, a 1-4 enables the source for all channels.
The Rev3 I400 has a relay gating the external HVPS output so that the initial voltage spike on this supply can be controlled.	PIC	When first enabled, both the external and signal HVPS outputs can spike to >10% of their full scale value, even if a low voltage is requested. When the External high voltage is changed from zero, an output relay is opened for 15 seconds, placing the device in the pending state, while the spike decays. Note that there is no similar protection for the signal voltage output. Generally the HVPS rating should be selected depending upon the application.

5/9/2007 FPGA 1.3 PIC 3.1

Problem/Feature	Module	Description
The monitor voltage does not work on the Rev3 I400.	PIC	Fixed.

12/3/2007 FPGA 1.3.3(For HW Rev2) FPGA 1.4.2(For HW Rev3) PIC 3.2F

Problem/Feature	Module	Description
The reset calibration does not properly reset the calibration.	PIC	Fixed.
The acquisition sometimes does not stop at the programmed TRIGger:POINts, instead rolling over to zero and starting over.	FPGA	Fixed.
Triggering needs to be standardized according to the standard for all integrating devices.	PIC	The trigger modes are now: 1) INTERNAL 2) EXTERNAL_START 3) EXTERNAL_GATED 4) MESSAGE 5) EXTERNAL_START_STOP These names are used in the ASCII commands. The changes from version 3.1 include (a) the addition of the EXTERNAL_STOP_START mode, which causes acquisition to start when the proper gate edge is received and stop when the gate returns to the original inactive state, and (b) the “GATED” ASCII keyword has been replaced with “EXTERNAL_GATED”. Finally, 0V causes the BNC gate sense to read low and 5V high.
The default reset and settle times are longer than they need to be.	PIC	The default reset time has been changed to 20us reset, 25us settle.

12/19/2007 FPGA 1.3.3(For HW Rev2) FPGA 1.4.2(For HW Rev3) PIC 3.2H

Problem	Module	Description
Weak pull-ups should be removed from port B.	PIC	Weak pull ups have been removed.
The MULL register was not being properly protected during the high priority interrupt.	PIC	Fixed. This probably had no effect on the operation of prior versions.

1/3/2008 FPGA 1.3.3(For HW Rev2) FPGA 1.4.2(For HW Rev3) PIC 3.2I

Problem	Module	Description
The “beacon message” bug needs to be applied to this version.	FPGA PIC	The fix has been applied to prevent unpredictable results that might be caused by the bug.

1/7/2008 FPGA 1.3.3(For HW Rev2) FPGA 1.4.2(For HW Rev3) PIC 3.2J

Problem	Module	Description
The communication lock-up fix reported for the I200 needs to be applied.	FPGA PIC	This has been traced to a communications state-machine problem which caused the device’s communications to lock up under some circumstances. This problem has been fixed by

		clearing the interrupt flag immediately after a message is read out of the FPGA buffer by the PIC.

1/18/2008 FPGA 1.3.3(For HW Rev2) FPGA 1.4.2(For HW Rev3) PIC 3.2K

Problem	Module	Description
I/O messages are sometimes lost by the A500 poll.	PIC	This problem was traced to the Initiate() function which shut off low priority interrupts while setting the FPGA registers. This was done due to a previous problem with interrupt register saving (now fixed) and is no longer necessary. Because interrupts were turned off, incoming messages were not properly serviced by the PSI engine, causing a timeout. Interrupts are no longer turned off.

9/15/2008 FPGA 1.3.3(For HW Rev2) FPGA 1.4.2(For HW Rev3) PIC 4.0A

Problem	Module	Description
Version number change for new A500 data acquisition.	PIC	This revision only implements a version number change in order to rev all PIC code to 4.0A for the new A500 data acquisition.