



Document Name <b>I3200 Version Notes</b>	System <b>I3200</b>	Developed for <b>General Distribution</b>
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### 1/09/2008 FPGA 5.3.5 PIC 3.1M

Problem	Module	Description
Initial release.		

### 1/18/2008 FPGA 5.3.5 PIC 3.10

Problem	Module	Description
I/O messages are sometimes lost by the A500 poll.	PIC	This problem was traced to the Initiate() function which shut off low priority interrupts while setting the FPGA registers. This was done due to a previous problem with interrupt register saving (now fixed) and is no longer necessary. Because interrupts were turned off, incoming messages were not properly serviced by the PSI engine, causing a timeout. Interrupts are no longer turned off.

### 3/25/2008 FPGA 5.3.14 PIC 3.2H

Problem	Module	Description
Fast data acquisition is needed for the I3200, at a minimum time-slice of 20 microseconds per 32x sample.		The FPGA and PIC code has been modified to enable this fast mode.

### 5/7/2008 FPGA 5.3.14 PIC 3.2I

Problem	Module	Description
The fiber-optic triggering for the optical gate is level triggered instead of edge triggered.		This has been change to edge triggered.

### 5/22/2008 FPGA 5.3.14 PIC 3.2J

Problem	Module	Description
Code for the Rev0 I3200 has been removed.		The I3200 Rev0 version has been established as a compile-time switch. Users of Rev0 should use 3.2K.

### 5/22/2008 FPGA 5.3.14 PIC 3.2K

Problem	Module	Description
Code for the Rev0 I3200 has been established with a compile time switch.		This version is equivalent to Rev 3.2J above, but is for exclusive use with the Revision 0 board.

### 6/2/2008 FPGA 5.3.14 PIC 3.2L

Problem	Module	Description
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When the programmable gain amplifier (PGA) is not set to 1, the integration time is not properly set to the displayed value.	PIC	This was due to a bug with the ConfigureGateInternalRange command, which was not properly accounting for the PGA value. Fixed.
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**6/27/2008 FPGA 5.3.15 PIC 3.2N**

Problem	Module	Description
SW1 cannot be set properly for lossless mode.	PIC	SW1 can now be set properly for lossless mode for integration times up to 60ms.
Message checksum errors occasionally occur when using fast mode.	FPGA	This was caused by the PIC writing it's 2 bytes (status, digital) asynchronously to the FPGA buffer while the FPGA was in the process of transmitting a message.
The device does not work on Mode 0 with the USB or A300.	PIC	Fixed.

**7/31/2008 FPGA 5.3.16 PIC 3.2P**

Problem	Module	Description
Messages are occasionally lost when running in fast message mode.	PIC	This has been traced to a problem with the PIC code which was erroneously asserting the FPGA transmit line when it thought a buffer lockup condition has occurred. Upon analysis and testing the buffer lockup code was found to be unnecessary and has been removed.
A problem exists with the old data flag returned in fast messages, causing messages between the I3200 and A500 to be corrupted with a checksum error.	FPGA PIC	This problem occurred when the PIC shut off the acquisition using the Trigger Control register while a fast message was in progress. The FPGA now implements a desired sample count that the PIC sets upon Initiate(). The FPGA thus shuts off the acquisition when the desired number of samples has been reached.

**9/12/2008 FPGA 5.3.17 PIC 4.0A**

Problem	Module	Description
Not all samples are properly acquired in buffered mode.	FPGA	The problem was traced to sample 1 which sometimes was a value from the previous acquisition with the new data flag set. This has been corrected.
Support for REV0 hardware is being dropped.	PIC	All references made to Revision 0 hardware has been eliminated.
The initiate command needs to have a "buffering" argument for the new A500 data acquisition.	PIC	The initiate command now takes a single byte argument – a 1 indicates that the I3200 should use internal buffering, and a 0 no internal buffering. This replaces the previous setting that was determined by the trigger points (buffer if NE Infinite).
The GATED trigger source is no longer offered as a feature.	PIC	This source has been removed.



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**3/23/2009 FPGA 5.3.17(HW REV 2<) FPGA 5.3.18(HW REV3) PIC 4.0E**

<b>Problem</b>	<b>Module</b>	<b>Description</b>
Support for the I3200 hardware rev 3 is needed.	FPGA PIC	Support for the new hardware version has been added. This includes support for <ul style="list-style-type: none"><li>• High voltage now controlled by FPGA, with more accurate ADC</li><li>• FPGA reprogramming from the host</li><li>• Support for a smaller calibration current for more accurate calibration</li></ul>
The trigger points should be limited to 65535 to match A500 capabilities.	PIC	The trigger points is now limited to 0xFFFF (65535). The value 0xFFFFFFFF is still sued to indicated infinite data collection.
FPGA uploads from the host is needed.	FPGA PIC	The FPGA program can now be transmitted from the host using the Pyramid diagnostic. From the Device tab, select the FPGA upload button, and select the appropriate .FHEX file.