



Document Name I200 Version Notes	System I200	Developed for General Distribution
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11/09/2007 FPGA 9.1.5 PIC 3.1C

Problem	Description
Initial release.	

12/03/2007 FPGA 9.1.5 PIC 3.1D

Problem	Description
For non-internally triggered modes, the current measured on channel 2 is incorrect.	Fixed – the setup time needs to be a minimum of 8 us, so the default has been changed.
The default reset and settle times are longer than they need to be.	The default reset time has been changed to 20us reset, 25us settle.

12/19/2007 FPGA 9.1.5 PIC 3.1F

Problem	Description
Weak pull-ups should be removed from port B.	Weak pull ups have been removed.
The MULL register was not being properly protected during the high priority interrupt.	Fixed. This probably had no effect on the operation of prior versions.

1/2/2008 FPGA 9.1.5 PIC 3.1H

Problem	Description
The setup value for capacitor#1 is occasionally corrupted upon power-up. This mostly appears to occur if the device has not been powered up for an extended period of time.	The source of this bug has not yet been located. A temporary fix has been installed that checks the setup in the foreground. The setup is reloaded if an error is detected. This fix will only be applied once after a powerup or Reset; after that a HardwareError is flagged requiring that the device be rebooted. Any time the fix is applied, both of the right side LEDs will be toggled for 1 second between green and red (they may appear yellow). This problem will be addressed in a future version of the firmware.

1/3/2008 FPGA 9.1.5 PIC 3.1I

Problem	Description
The setup value for capacitor#1 is occasionally corrupted upon power-up. This mostly appears to occur if the device has not been powered up for an extended period of time.	This bug has been traced to the beacon message that is automatically transmitted by a device after not receiving a message on the fiber loop for >5sec. This problem has been fixed.

1/7/2008 FPGA 9.1.5 PIC 3.1J

Problem	Description
When operating with the A500,	This has been traced to a communications state-machine



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communication fails when interrogating the device at full rate.	problem which caused the device's communications to lock up under some circumstances. This problem has been fixed by clearing the interrupt flag immediately after a message is read out of the FPGA buffer by the PIC.
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1/18/2008 FPGA 9.1.5 PIC 3.1K

Problem	Description
I/O messages are sometimes lost by the A500 poll.	This problem was traced to the Initiate() function which shut off low priority interrupts while setting the FPGA registers. This was done due to a previous problem with interrupt register saving (now fixed) and is no longer necessary. Because interrupts were turned off, incoming messages were not properly serviced by the PSI engine, causing a timeout. Interrupts are no longer turned off.

3/31/2008 FPGA 9.1.7 PIC 3.2B

Problem	Description
Fast data acquisition is needed for the I200, at a minimum time-slice of 20 microseconds per 32x sample.	The FPGA and PIC code has been modified to enable this fast mode.

5/9/2008 FPGA 9.1.7 PIC 3.2C

Problem	Description
The fiber-optic triggering for the optical gate is level triggered instead of edge triggered.	This has been change to edge triggered.