



Document Name F100 Version Notes	System F100	Developed for General Distribution
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12/07/2007 FPGA 6.2.3 PIC 3.0N

Problem	Module	Description
Initial release.		

12/18/2007 FPGA 6.2.3 PIC 3.0O

Problem	Module	Description
Weak pull-ups should be removed from port B.	PIC	Weak pull ups have been removed.
The MULL register was not being properly protected during the high priority interrupt.	PIC	Fixed. This probably had no effect on the operation of prior versions.

1/03/2008 FPGA 6.2.3 PIC 3.0P

Problem	Module	Description
The "beacon message" bug needs to be applied to this version.	PIC	The fix has been applied to prevent unpredictable results that might be caused by the bug.

1/1/2008 FPGA 6.2.3 PIC 3.0Q

Problem	Module	Description
The communication lock-up fix reported for the I200 needs to be applied.	PIC	This has been traced to a communications state-machine problem which caused the device's communications to lock up under some circumstances. This problem has been fixed by clearing the interrupt flag immediately after a message is read out of the FPGA buffer by the PIC.

1/10/2008 FPGA 6.2.3 PIC 3.0R

Problem	Module	Description
An option to run at a 20mA range must be added.	PIC	A 20mA range option has been added to the F100. See the jumper settings application note for details.

4/20/2008 FPGA 6.2.3 PIC 3.0S

Problem	Module	Description
An option to run at the lowest range only is required.	PIC	Jumper 7 now fixes the F100 to operate uniquely at the 1 microampere range (range 1). The unit will calibrate normally.



F400 Version Notes

7/01/2008 FPGA 6.2.5 PIC 3.0T

Problem	Module	Description
Special fast messages are needed that read the integrated dose.	FPGA	A new fast message has been added that reads the integrated binary dose since the last read message. The number of 4us samples taken is also returned so that the current can be computed.
A programmable dosimetry gate is needed.	FPGA	A new feature has been added that allows a target dose to be loaded to the FPGA. After receiving this dose, the FPGA will assert a digital line until that dose as been observed, at which point the digital line is dropped low.
Messages are occasionally lost when running in fast message mode.	PIC	This has been traced to a problem with the PIC code which was erroneously asserting the FPGA transmit line when it though a buffer lockup condition has occurred. Upon analysis and testing the buffer lockup code was found to be unnecessary and has been removed.

9/22/2008 FPGA 6.2.8 PIC 4.0A

Problem	Module	Description
Support is need for the Revision-2 hardware. Specifically, the HVPS is now controlled and read back by the FPGA instead of the PIC.	FPGA PIC	The HVPS control and readback is now completely controlled by the FPGA.
A feature is needed to apply a user offset to each ADC value.	PIC	A new command has been added that allows the host to transmit a user offset to the F100 that will be subtracted from each ADC value. This offset is in addition to the calibration offset current supported by the device.
A charge monitor feature is needed that will output a pulse each time a predefined charge aliquot is observed.	FPGA PIC	A new command has been added that allows the host to download a charge aliquot to the F100. Each time the F100 detects this amount of charge, a short pulse is transmitted on one of its digital outputs. This integrated charge value is not allowed to wind up in the direction opposite in polarity to the programmed value.
A 2000VDC HVPS needs to be supported.	PIC	A new jumper setting has been added that programs the F100 for a 2000VDC HVPS.
The restriction for "enhanced mode" that limits to range #1 needs to be removed so that the unit tests can pass.	PIC	This restriction has been removed. Applications that depend on this should check the range before executing critical code.
Automatic FPGA download is needed.	FPGA	Support has been added for the FPGA download. This has not been tested.
The charge monitor winds up when negative values are present.	FPGA	Negative values continue to be integrated, but the integral is never allowed to go negative.

11/12/2008 FPGA 6.2.8 PIC 4.0C

Problem	Module	Description
The calibration is not completely	PIC	Fixed. The offset was being subtracted twice



F400 Version Notes

accurate.		when computing the gain. Also, the offset is now subtracted as a floating value to get more accurate gains.
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1/15/2009 FPGA 6.2.8 PIC 4.0D

	Module	Description
Support for the 200ma range is needed.	PIC	A new jumper option has been added to support the 200ma range. The range settings for the top 4 ranges are now 400, 200, 80, and 40 mA.

1/30/2009 FPGA 6.2.9 PIC 4.0E

	Module	Description
Option bit #8 cannot be read by the PIC.	FPGA	This has been fixed. Previously in REV1 hardware this bit was used to drive the enhanced mode dosimetry signal.
Range 16 is 400mA, but the device cannot read 400mA.	PIC	When the 200mA jumper selection is made, the highest range, 400mA, is suppressed.
Support is needed for the relay input that gates two current signals together.	PIC	A new command has been added named RelayCombine which switches the relay that combines two incoming currents into the single input channel. This feature uses the same digital used for the external calibration. Option bit #8 now controls which of these two features is active (this is a board population issue). When the jumper is out, the output is used for external calibration, as before. When present, the output is used to combine the signals.
An ASCII command is needed to support the new RelayCombine feature.	PIC	The existing command RELAY:ACTuator has been removed. The actuator is now set with RELay:ACTuator. A new command has been added to set the combine state called RELAY:COMbine. The state of both relays is read back using RELay?, which returns a single integer, where bit0 set = actuator set, bit 1 set = combiner set.

2/09/2009 FPGA 6.2.12 PIC 4.0F

	Module	Description
Support for the F100 hardware rev 3 is needed.	FPGA PIC	Support for the new hardware version has been added. This includes support for <ul style="list-style-type: none"> FPGA reprogramming from the host
FPGA uploads from the host is needed.	FPGA PIC	The FPGA program can now be transmitted from the host using the Pyramid diagnostic. From the Device tab, select the FPGA upload button, and select the appropriate .FHEX file.